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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,799	02/09/2004	Perry Scott Lorenz	08211/0200372-US0/P05790	9070

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EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/774,799	LORENZ, PERRY SCOTT	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/25/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-3, 5-11 and 13-20 rejected under 35 U.S.C. 102(b) as being anticipated by Azimi et al. (US 6163183).

With respect to claim 1, figure 3 of Azimi et al. (US 6163183) discloses a circuit for temperature sensing, comprising: a comparator circuit (20) that is arranged to provide a trigger signal by comparing a reference signal (25) to a temperature sensor signal (24); a gate circuit (10) that is arranged to provide an output signal (100) by gating a gate input signal (12) subject to control by a gate Control signal, wherein the gate input signal is based at least in part on the trigger signal, and wherein the gate control signal is based at least in part on a power-on-reset signal (120); and a hysteresis-and-output-sensor circuit (32 and 34) that is configured to control the reference signal in response to a sensed signal, wherein the sensed signal is based at least in part on the output signal.

With respect to claim 2, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, wherein the power-on-reset (120) signal is the gate control signal.

With respect to claim 3, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, further comprising: a timer circuit (36 and 38) that is configured to provide a

mute signal in response to the power-on-reset signal (120), wherein the mute signal is the gate control signal.

With respect to claim 5, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, wherein the sensed signal is the output signal (100), and wherein the gate input signal is the trigger signal (12).

With respect to claim 6, figure 3 of Azimi et al. (US 6163183) the circuit of Claim 1, wherein the gate circuit is configured to provide the output signal such that a logic level of the output signal (100) corresponds to a logic level of the trigger signal (12) if the gate control signal corresponds to an inactive level, and the logical level of the output signal (100) corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 7, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, wherein the gate circuit includes an AND gate (10).

With respect to claim 8, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, wherein the comparator circuit (20) is configured to provide the trigger signal such that the trigger signal corresponds to a first logic level if a voltage associated with the reference signal is greater than a voltage associated with the temperature sensor signal (22), and the trigger corresponds to a second logic level if the voltage associated with the reference signal is less than the temperature sensor signal (22).

With respect to claim 9, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, further comprising: a reference circuit (producing Vmonitor) that is configured to provide the reference signal in conjunction with the hysteresis-and-output-

sensor circuit (32 and 34), wherein the hysteresis-and-output-sensor circuit is arranged to modify the reference signal if the hysteresis-and-output-sensor circuit is enabled, and wherein the hysteresis-and-output-sensor circuit is disabled if the output signal corresponds to a first logic level.

With respect to claim 10, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 9, wherein the reference circuit includes: a resistor (30) that is coupled to the hysteresis-and-output-sensor circuit (32 and 34) and the comparator circuit (20); and a current source circuit (38) that is configured to provide a current to the resistor.

With respect to claim 11, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 10, wherein the hysteresis-and-output-sensor circuit (32 and 34) is configured to provide a hysteresis current to the resistor (30) if the output signal corresponds to the second logic level.

With respect to claim 13, figure 3 of Azimi et al. (US 6163183) discloses a method for temperature sensing, comprising: activating hysteresis (via 34) if a temperature-sensing condition has occurred; and ensuring that the hysteresis is automatically inactive (via 38 or 120) when the circuit is powering up.

With respect to claim 14, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 13, further comprising providing a reference signal (25), wherein activating the hysteresis includes modifying the reference signal (via 34), and wherein the hysteresis is active if the output signal corresponds to a first logic level.

With respect to claim 15, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 13, wherein ensuring includes providing an output signal (100) in

response to a gate input signal (12) and a gate control signal (14), wherein the gate control signal is derived form a power-on-reset signal (120), a logic level of the output signal (16) corresponds to a logic level of the gate input signal (12) if the gate control signal corresponds to an inactive level, and the logical level of the output signal corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 16, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 15, furthering comprising: comparing a temperature sensor signal (24) to a reference signal (25); and providing a trigger signal in response to the comparison, wherein the gate input signal (12) is based at least in part on the trigger signal.

With respect to claim 17, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 15, wherein providing the output signal includes performing a logical AND function (10) on the gate input signal (12) and the gate control signal (14).

With respect to claim 18, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 15, further comprising: applying a power supply signal; and providing the gate control signal in response to the power-on-reset signal (120), wherein providing the gate control signal (12) includes: providing the gate control signal such that the gate control signal corresponds to an active logic level when the power supply signal is initially applied, and for a pre-determined period of time thereafter; and providing the gate control signal such that the gate control signal corresponds to an inactive level after the pre-determined period of time.

With respect to claim 19, figure 1 of Azimi et al. (US 6163183) discloses the method of Claim 15, further comprising: providing a first current; and converting a

reference current into the reference signal (25), wherein activating the hysteresis includes: providing a hysteresis current if the output signal corresponds to a first logic level; providing substantially no current if the output signal corresponds to a second logic level; and providing the reference current by combining the first current and the hysteresis current.

With respect to claim 20, figure 3 of Azimi et al. (US 6163183) discloses a circuit for temperature sensing, comprising: means for activating hysteresis (32, 34 and 38) if a temperature-sensing condition has occurred; and means for ensuring that the hysteresis is automatically inactive when the circuit is powering up (input from 120).

3. Claim 1-3 and 5-11 and 13-20 rejected under 35 U.S.C. 102(b) as being anticipated by Lim et la. (US 5614857)

With respect to claim 1, figure 4 of Lim et al. (US 5614857) discloses a circuit for temperature sensing, comprising: a comparator circuit (20) that is arranged to provide a trigger signal by comparing a reference signal (Vth) to a temperature sensor signal (Vin2); a gate circuit (AND45) that is arranged to provide an output signal (Vout2) by gating a gate input signal (input at AND45) subject to control by a gate Control signal, wherein the gate input signal is based at least in part on the trigger signal, and wherein the gate control signal is based at least in part on a power-on-reset signal (Vin1); and a hysteresis-and-output-sensor circuit (R41, R42 and Q41) that is configured to control the reference signal in response to a sensed signal, wherein the sensed signal is based at least in part on the output signal.

With respect to claim 2, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, wherein the power-on-reset (Vin1) signal is the gate control signal.

With respect to claim 3, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, further comprising: a timer circuit (30) that is configured to provide a mute signal in response to the power-on-reset signal (Vin1), wherein the mute signal is the gate control signal.

With respect to claim 5, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, wherein the sensed signal is the output signal (vout2), and wherein the gate input signal is the trigger signal.

With respect to claim 6, figure 4 of Lim et al. (US 5614857) the circuit of Claim 1, wherein the gate circuit is configured to provide the output signal such that a logic level of the output signal (Vout2) corresponds to a logic level of the trigger signal if the gate control signal corresponds to an inactive level, and the logical level of the output signal (Vout2) corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 7, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, wherein the gate circuit includes an AND gate (AND45).

With respect to claim 8, figure 4 Lim et al. (US 5614857) discloses the circuit of Claim 1, wherein the comparator circuit (20) is configured to provide the trigger signal such that the trigger signal corresponds to a first logic level if a voltage associated with the reference signal is greater than a voltage associated with the temperature sensor signal (Vin2), and the trigger corresponds to a second logic level if the voltage

associated with the reference signal is less than the temperature sensor signal (Vin2).

With respect to claim 9, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, further comprising: a reference circuit (R45 and Q45) that is configured to provide the reference signal in conjunction with the hysteresis-and-output-sensor circuit (R41, R42 and Q41), wherein the hysteresis-and-output-sensor circuit is arranged to modify the reference signal if the hysteresis-and-output-sensor circuit is enabled, and wherein the hysteresis-and-output-sensor circuit is disabled if the output signal corresponds to a first logic level.

With respect to claim 10, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 9, wherein the reference circuit includes: a resistor (R45) that is coupled to the hysteresis-and-output-sensor circuit (R41, R42 and Q41) and the comparator circuit (20); and a current source circuit (Q45) that is configured to provide a current to the resistor.

With respect to claim 11, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 10, wherein the hysteresis-and-output-sensor circuit (R41, R42 and Q41) is configured to provide a hysteresis current to the resistor (R45) if the output signal corresponds to the second logic level.

With respect to claim 13, figure 4 of Lim et al. (US 5614857) discloses a method for temperature sensing, comprising: activating hysteresis (via Q41) if a temperature-sensing condition has occurred; and ensuring that the hysteresis is automatically inactive (via 30) when the circuit is powering up.

With respect to claim 14, figure 4 of Lim et al. (US 5614857) discloses the

method of Claim 13, further comprising providing a reference signal (Vth), wherein activating the hysteresis includes modifying the reference signal (via Q41), and wherein the hysteresis is active if the output signal corresponds to a first logic level.

With respect to claim 15, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 13, wherein ensuring includes providing an output signal (Vout2) in response to a gate input signal (Vout2) and a gate control signal (Vout1), wherein the gate control signal is derived form a power-on-reset signal (Vin1), a logic level of the output signal (Vout2) corresponds to a logic level of the gate input signal (Vout2) if the gate control signal corresponds to an inactive level, and the logical level of the output signal corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 16, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 15, furthering comprising: comparing a temperature sensor signal (Vin2) to a reference signal (Vth); and providing a trigger signal in response to the comparison, wherein the gate input signal is based at least in part on the trigger signal.

With respect to claim 17, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 15, wherein providing the output signal includes performing a logical AND function (AND45) on the gate input signal (Vout2) and the gate control signal (Vout1).

With respect to claim 18, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 15, further comprising: applying a power supply signal; and providing the gate control signal in response to the power-on-reset signal (Vin1), wherein

providing the gate control signal (Vout1) includes: providing the gate control signal such that the gate control signal corresponds to an active logic level when the power supply signal is initially applied, and for a pre-determined period of time thereafter; and providing the gate control signal such that the gate control signal corresponds to an inactive level after the pre-determined period of time.

With respect to claim 19, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 15, further comprising: providing a first current (through Q45); and converting a reference current into the reference signal (Vth), wherein activating the hysteresis includes: providing a hysteresis current if the output signal corresponds to a first logic level; providing substantially no current if the output signal corresponds to a second logic level; and providing the reference current by combining the first current and the hysteresis current.

With respect to claim 20, figure 4 of Lim et al. (US 5614857) discloses a circuit for temperature sensing, comprising: means for activating hysteresis (Q41) if a temperature-sensing condition has occurred; and means for ensuring that the hysteresis is automatically inactive when the circuit is powering up (input from Vin).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Azimi et al. (US 6163183) in view of Nakajima et al. (US 6417704).

With respect to claim 4, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 3, but fails to disclose the detail of circuit that generates the reset signal. However, Nakajjima et al.'s figure 1 shows a reset signal generation circuit in response to the circuit power supply and having low power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use Nakajima et al.'s reset circuit to generate Azimi et al.'s reset signal for the purpose of saving power consumption. It is further noted that it is seen as an obvious design preference to select Nakajima et al.'s output signal or its complemented signal as the reset signal dependent on a particular environment of use to ensure optimum performance. Thus the modified Azimi et al.'s circuit further shows that the timer circuit includes a one-shot timer circuit (Nakajima et al.'s 12), wherein the one-shot timer circuit is configured to provide the mute signal such that the gate control signal such that the mute signal corresponds to an active logic level when a power supply signal is applied to the circuit, and for a pre-determined period of time thereafter; and such that the mute signal corresponds to an inactive level after the pre- determined period of time.

6. With respect to claim 12, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 10, but fails to disclose wherein a resistance that is associated with the resistor (30) is adjustable. It is well know to use an adjustable resistor to optimize resistance values in a circuit. It would have been obvious at the time the invention was

made to a person having ordinary skill in the art to substitute the resistor (30) in Azimi et al. with a variable resistor for the purpose of optimizing resistance.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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PRIMARY EXAMINER
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